IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of	**MAIL STOP AF**
Gregory S. Andre et al.	Group Art Unit: 2611
Application No.: 09/955,966	Examiner: SAM K AHN
Filed: September 20, 2001	Confirmation No.: 1908
For: SYSTEM BUS TRANSCEIVER INTERFACE	

PRE-APPEAL BRIEF REQUEST FOR REVIEW

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In response to the Office Action dated April 3, 2007, a Notice of Appeal is filed herewith, and a Pre-Appeal Conference is requested to review the above-identified application. No amendments are being filed with this request. For at least the following reasons, the rejections raised in the Final Office Action are clearly improper and without basis.

OVERVIEW

Independent claim 1 is allowable over the combination of U.S. Patent 6,609,167 (Bastiani et al.) and U.S. Patent 6,718,413 (Wilson et al.). For the like reasons, dependent claim 9 is allowable over the combination of the Bastiani et al. patent; the Wilson et al. patent; and U.S. Patent 5,555,430 (Gephardt et al.). These documents, when considered individually or in the various combinations suggested by the Examiner, do not teach or suggest Appellants' below recited claim features. Independent claim 1 is therefore allowable.

ARGUMENT

1. The Examiner Has Failed To Establish A Prima Facie Case of Obviousness In Combining The Bastiani et al. Patent And The Wilson et al. Patent To Reject Independent Claim 1

As set forth of record in the March 7, 2007 Amendment, Appellants have disclosed a transceiver configured for use with a multi-tier system bus (e.g., paragraph [0015). For example, in Fig. 2, a bus interface utilizes a transmitter and receiver that operate between the local processor bus 202 and the system bus or module bus 204. The bus 204 can be either a system bus 102 or a module bus 122 as shown in Figure 1. The local processor bus 202 can be a bus connecting a bus interface device 128 to components within the same node of the module, such as processors and memory, or, in the case of the sensor interface, internal processors and memory (e.g., paragraph [0084]). Two basic types of operations are supported, including DMA operations and control operations (e.g., paragraph [0093]).

The foregoing features are broadly encompassed by claim 1, which recites a transceiver for use within a multi-tier system bus configuration, including, among other features, means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations for forward to a local processor bus; and means for buffering instructions transmitted via the local processor bus to provide a separate transmit buffering of control actions from DMA operations to be transmitted to the system bus; wherein access to the multi-tier system bus is arbitrated such that control actions preempt DMA operations.

Bridging pages 2 and 3 of the final Office Action, the Examiner maintains that the Bastiani et al. patent teaches "means for buffering instructions received and transmitted...via the system bus...to provide a separate buffering of control actions...from DMA operations." To reinforce this notion, bridging pages 3 and 4 of the final Office Action, the Examiner further asserts that "And further, the buffering instructions explained above, are transmitted and received between the Tx Rx 372 and PCI Interface 352 in Fig. 41, which are coupled to the ASP Bus (wherein this bus is interpreted as a local processor bus) and the system bus (164 in Fig. 10), respectively." Appellants respectfully disagree with the Examiner's ultimate conclusion.

As argued in Appellants' March 7, 2007 Remarks, the Bastiani et al. patent does not relate to a transmitter and receiver that operate between a local processor bus and a system bus. Rather, what is shown in Fig. 41 of the Bastiani et al. patent is an advanced serial protocol (ASP) controller connected between a PCI interface (352) on one side, and a plurality of serial transceivers (372). These transceivers (372) are ENDEC transceivers for serial data transmission (col. 48. lines 62-65). There is no teaching or a suggestion of at least 1) a transceiver described within a multi-tier system bus having a local processor bus and a system bus; and there is no suggestion of 2) a separate buffering of control actions from DMA operations within such a multi-tier system bus architecture. The Bastiani et al. patent would not have taught or suggested specifically means for buffering instructions received via the system bus to provide a separate receive buffering of control actions from direct memory access (DMA) operations for forward to a local processor bus; and means for buffering instructions transmitted via the local processor bus to provide a

separate transmit buffering of control actions from DMA operations to be transmitted to the system bus, as recited in claim 1.

Further, as admitted by the Examiner on page 4 of the final Office Action, the Bastiani et al. patent "does not explicitly teach wherein access to the multi-tier system bus is arbitrated such that control actions preempt DMA operations." The Wilson et al. patent is therefore relied upon in the Examiner's initial combination of documents for the recited feature. However, the Wilson et al. patent does not cure the deficiencies of the Bastiani et al. patent. As set forth in Appellants' March 7, 2007 and November 27, 2006 Remarks of record, the Wilson et al. patent merely relates to SCSI devices contending for a bus in operation 606 to allow one SCSI device to transfer data to the host adapter in the operation 614 (col. 10, lines 57-65). The Wilson et al. patent would not have taught or suggested at least the above-recited claim features.

Moreover, there would have been no motivation or suggestion to have combined the references in the manner suggested by the Examiner. The Bastiani et al. patent discloses an ASP controller connected between a PCI interface and serial transceivers. In contrast, the Wilson et al. disclosure relates to contention-based methods for generating reduced number of interrupts. Neither of the two applied references specifically relate to an arbitration involving access to a multi-tier system bus such that control actions preempt DMA operations.

At least for the foregoing reasons, Appellants' claim 1 is allowable. The remaining claims depend from independent claim 1 and recite additional advantageous features which further distinguish over the documents relied upon by the Examiner. As such, the present application is in condition for allowance.

2. The Examiner Has Failed To Establish A Prima Facie Case of Obviousness In Combining The Bastiani et al. Patent, The Wilson et al. Patent and The Gephardt et al. Patent To Reject Dependent Claim 9

As argued of record in the March 7, 2007 Remarks, the Gephardt et al. patent does not cure the deficiencies of the Bastiani et al. patent and the Wilson et al. patent. The Gephardt et al. patent was applied for its disclosure of interrupt management in a multiprocessing system (col. 22, line 61 through col. 23, line 17). However, the Gephardt et al. patent would not have taught or suggested the above recited claim features.

Claim 9 depends from claim 1. Claim 9 is therefore allowable.

CONCLUSION

The Examiner has not established a prima facie case of obviousness in combining the references used to reject claims 1-9. A reversal of the final rejection, and allowance of the present application, are therefore requested.

Respectfully submitted,

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Date: July 2, 2007

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